

S/N 09/955,270

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT RECEIVED

Applicant: Christophe J. Chevallier
Serial No.: 09/955,270
Filed: September 18, 2001
Title: SUPPLY VOLTAGE REDUCTION CIRCUIT FOR INTEGRATED CIRCUIT

Examiner: Edward Wojciechowicz

Group Art Unit: 2815

Docket: 703.019US3

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TECHNOLOGY CENTER 2800

Commissioner for Patents
Washington, D.C. 20231

In response to the Office Action mailed on October 16, 2002, please amend the above-identified patent application as follows.

IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. The substitute claim set is intended to reflect amendment of previously pending claims 22, 27-28, 34, 38, 41, 45, 49, 52, 61, 63, 65, 69, 72, and 75. The specific amendments to individual claims are detailed in the following marked up set of claims.

22. (Amended) A method of reducing a voltage, comprising:
applying the voltage to a transistor;
reducing the voltage by a threshold voltage of the transistor; and
providing the voltage reduced by [a] the threshold voltage of the transistor at an output of the transistor, wherein the output of the transistor is coupled to a well that bounds the transistor.

27. (Amended) A method of reducing a voltage, comprising:
applying the voltage to a first source/drain and a gate of a transistor;
reducing the voltage by a threshold voltage of the transistor; and
providing the voltage reduced by [a] the threshold voltage of the transistor at a second source/drain of the transistor and a well bounding the transistor.

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